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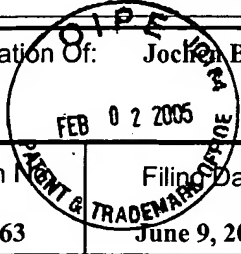
# TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

(Under 37 CFR 1.97(b) or 1.97(c))

Docket No.

FIS920040005US1

In Re Application Of: Jochen Beintner, et al.



Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/709,963	June 9, 2004	Unassigned	23389	2812	3962

Title: **RAISED STI PROCESS FOR MULTIPLE GATE OX AND SIDEWALL PROTECTION ON STRAINED SI/SGOI STRUCTURE WITH ELEVATED SOURCE/DRAIN**

Address to:

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

## 37 CFR 1.97(b)

1. ☒ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

## 37 CFR 1.97(c)

2. ☐ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:
- ☐ the statement specified in 37 CFR 1.97(e);
- OR**
- ☐ the fee set forth in 37 CFR 1.17(p).

## TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

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## Payment of Fee

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

- ☐ A check in the amount of \_\_\_\_\_ is attached.
- ☒ The Director is hereby authorized to charge and credit Deposit Account No. 09-0458/IBM as described below.
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Leslie S. Szivos, Ph.D. Reg. No. 39,394	
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Dated: January 27, 2005

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**Applicant(s):** Jochen Beintner, et al.      **Examiner:** Unassigned

**Serial No:** 10/709,963      **Art Unit:** 2812

**Filed:** June 9, 2004      **Docket:** FIS920040005US1 (17369)

**Dated:** January 27, 2005

**For:** RAISED STI PROCESS FOR MULTIPLE GATE OX AND SIDEWALL PROTECTION ON STRAINED Si/SGOI STRUCTURE WITH ELEVATED SOURCE/DRAIN

**INFORMATION DISCLOSURE STATEMENT**

Sir:

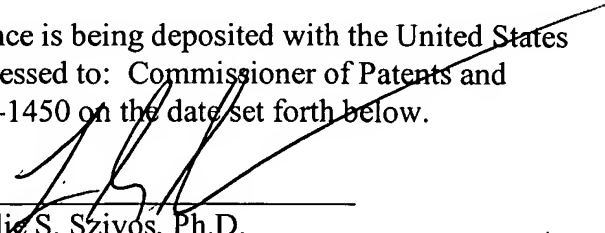
Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, applicants submit the following references which applicants believe may be material to the above-identified patent application. A copy of the references which applicants wish to make of record in this case is enclosed herein for the Examiner's convenience along with a listing on Form PTO-1449 attached.

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**CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)**

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Dated: January 27, 2005

  
\_\_\_\_\_  
Leslie S. Szivos, Ph.D.

1. U.S. Patent No. 3,602,841, dated August 31, 1971, issued to McGroddy;
2. U.S. Patent No. 4,665,415, dated May 12, 1987, issued to Esaki, et al.;
3. U.S. Patent No. 4,853,076, dated August 1, 1989, issued to Tsaur, et al.;
4. U.S. Patent No. 4,855,245, dated August 8, 1989, issued to Neppl, et al.;
5. U.S. Patent No. 4,952,524, dated August 28, 1990, issued to Lee, et al.;
6. U.S. Patent No. 4,958,213, dated September 18, 1990, issued to Eklund, et al.;
7. U.S. Patent No. 5,006,913, dated April 9, 1991, issued to Sugahara, et al.;
8. U.S. Patent No. 5,060,030, dated October 22, 1991, issued to Hoke;
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14. U.S. Patent No. 5,371,399, dated December 6, 1994, issued to Burroughes, et al.;
15. U.S. Patent No. 5,391,510, dated February 21, 1995, issued to Hsu, et al.;
16. U.S. Patent No. 5,459,346, dated October 17, 1995, issued to Asakawa, et al.;

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19. U.S. Patent No. 5,561,302, dated October 1, 1996, issued to Candelaria;
20. U.S. Patent No. 5,565,697, dated October 15, 1996, issued to Asakawa, et al.;
21. U.S. Patent No. 5,571,741, dated November 5, 1996, issued to Leedy, et al.;
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23. U.S. Patent No. 5,592,018, dated January 7, 1997, issued to Leedy;
24. U.S. Patent No. 5,670,798, dated September 23, 1997, issued to Schetzina;
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31. U.S. Patent No. 5,946,559, dated August 31, 1999, issued to Leedy;
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35. U.S. Patent No. 6,025,280, dated February 15, 2000; issued to Brady, et al.;
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39. U.S. Patent No. 6,107,143, dated August 22, 2000, issued to Park, et al.;
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58. U.S. Patent No. 6,403,975, dated June 11, 2002, issued to Brunner, et al.;
59. U.S. Patent No. 6,406,973, dated June 18, 2002, issued to Lee;
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61. U.S. Patent No. 6,476,462, dated November 5, 2002, issued to Shimizu, et al.;
62. U.S. Patent No. 6,493,497, dated December 10, 2002, issued to Ramdani, et al.;
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90. European Patent Application Publication No. EP 1 174 928 A1, dated 01/23/02, issued to Hitachi Ltd.;
91. European Patent Application Publication No. EP 0 967 636 A2, dated 12/29/1999, issued to Rengarajan, et al.;

92. International Patent Application Publication No. WO 02/454156 A2, dated 06/06/2002, issued to Armstrong et al.;

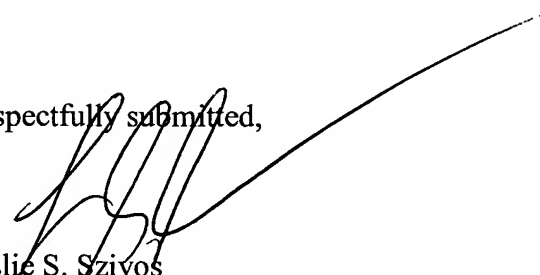
93. International Application Publication No. WO 94/27317, dated 05/06/1993, issued to Winnerl, et al.;

Applicant is submitting copies of the above-cited non-U.S. Patent references.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no statement or fee is required.

In accordance with the waiver of 37 C.F.R. § 1.98 (a)(2)(i), per 1276 OG 55, August 5, 2003, applicants are not required to submit copies of the above-cited U.S. Patent references.

Respectfully submitted,

  
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U.S. DEPARTMENT OF COMMERCE  
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STATEMENT BY APPLICANT

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(Use several sheets if necessary)

ATTY. DOCKET NO.  
FIS920040005US1 (17369)SERIAL NO.  
10/709,963APPLICANTS  
Jochen Beintner, et al.FILING DATE  
June 9, 2004GROUP ART UNIT  
2812

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	3,602,841	08/31/71	McGroddy			
	4,665,415	05/12/87	Esaki, et al			
	4,853,076	08/01/89	Tsaur, et al			
	4,855,245	08/08/89	Neppl, et al			
	4,952,524	08/28/90	Lee, et al			
	4,958,213	09/18/90	Eklund, et al			
	5,006,913	04/09/91	Sugahara, et al			
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	5,108,843	04/28/92	Ohtaka, et al			
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	5,354,695	10/11/94	Leedy			
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	5,571,741	11/05/96	Leedy, et al			
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	5,840,593	11/24/98	Leedy			
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Examiner

Date Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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APPLICANTS

Jochen Beintner, et al.

FILING DATE

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GROUP ART UNIT

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		5,940,736	08/17/99	Brady, et al			
		5,946,559	08/31/99	Leedy			
		5,960,297	09/28/99	Saki			
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		6,362,082	03/26/02	Doyle, et al			
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		6,461,936	10/18/02	Von Ehrenwall			
		6,476,462	11/05/02	Shimizu, et al			

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		6,493,497	12/10/02	Ramdani, et al			
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		6,531,740	03/11/03	Bosco, et al			

## U.S. PATENT APPLICATION PUBLICATION DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		2001/000978 4 A1	07/26/01	Ma, et al			
		2002/007459 8 A1	07/20/02	Doyle, et al			
		2002/008647 2 A1	07/04/02	Roberds, et al			
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		2003/005718 4 A1	03/27/03	Yu, et al			
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(REV. 7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEAtty. Docket No.  
FIS920040005US1 (17369)Serial No.  
10/709,963**LIST OF PRIOR ART  
CITED BY APPLICANT**

(Use several sheets if necessary)

Applicants  
Jochen Beintner, et al.Filing Date  
June 9, 2004Group  
2812**FOREIGN PATENT DOCUMENTS**

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
		EPO 01/62362	26/06/89	Europe				
		EP 1 174 928 A1	01/23/02	Europe				
		EP 0 967 636 A2	12/29/1999	Europe				
		WO 02/454156 A2	06/06/2002	PCT				
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**OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

		Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si n-MOSFETs", International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998
		Rim, et al. "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs", 2002 Symposium On VLSI Technology Digest of Technical Papers, IEEE, pp 98-99
		Scott, et al. "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", International Electron Devices Meeting, 34.4.1, IEEE, September 1999
		Ootsuka, et al. "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Application", International Electron Device Meeting, 23.5.1, IEEE, April 2000
		Ito, et al. "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design", International Electron Devices Meeting, 10.7.1, IEEE, April 2000
		Shimizu, et al. "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement", International Electron Devices Meeting, IEEE, March 2001
		Ota, et al. "Novel Locally Strained Channel Technique for high Performance 55nm CMOS", International Electron Devices Meeting, 2.2.1, IEEE, February 2002
		Ouyang, et al. "Two-Dimensional Bandgap Engineering in a Novel Si/SiGe pMOSFETs With Enhanced Device Performance and Scalability", Microelectronics Research Center, pp 151-154, 2000 IEEE
		Sayama et al., "Effect of <Channel Direction for High Performance SCE Immune pMOSFET with Less Than 0.15um Gate Length" ULSI Development Center, pp27.5.1-27.5.4, 1999 IEEE

EXAMINER

DATE CONSIDERED

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